

- 4 which has an edge;
5 forming a conductive strip along the edge of the bond shelf; and
6 removing a portion of the conductive strip.

- 1 14. The method as recited in claim 13, wherein
2 the conductive strip is formed by plating a conductive material
3 onto the edge.

- 1 15. The method as recited in claim 13, wherein
2 the portion of the conductive strip is removed by
3 drilling a portion of the bond shelf.

- 1 16. The method as recited in claim 13, further comprising:
2 mounting an integrated circuit to the housing and connecting the
3 integrated circuit to the bond pad.

- 1 17. The method as recited in claim 13, wherein
2 the portion of the conductive strip is removed by
3 etching away a portion of a conductive material on the bond
4 shelf.

- 1 18. The method as recited in claim 13, wherein
2 the conductive strip is formed along the edge of the bond shelf
3 by

4 masking all surfaces except for the edge of the bond shelf, and
5 plating a conductive material onto the edge of the bond shelf.

1 19. The method as recited in claim 18, wherein
2 the conductive material is copper, and
3 the conductive strip is further formed by
4 plating gold onto the copper.

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1 20. The method as recited in claim 19, wherein
2 the portion of the conductive strip is removed by
3 drilling a portion of the bond shelf.

1 21. A method of forming an integrated circuit package,
2 comprising:
3 providing a package housing having a first plurality of bonding
4 pads located on a first bond shelf, the first bond shelf having
5 a first edge;
6 forming a first conductive strip along the first edge of the
7 first bond shelf, the first conductive strip wrapping around the
8 edge of the first bond shelf from at least one of the first
9 plurality of bonding pads on the first bond shelf to a first
10 conductor under the first bond shelf; and,
11 removing a portion of the first conductive strip.

1 22. The method as recited in claim 21, wherein
2 the first conductive strip is formed by plating a conductive
3 material onto the first edge.

1 23. The method as recited in claim 21, wherein
2 the first conductor under the first bond shelf is a power bus.

1 24. The method as recited in claim 21, wherein
2 the first conductor under the first bond shelf is a routing
3 trace.

1 25. The method as recited in claim 21, wherein
2 the portion of the first conductive strip is removed by
3 drilling a portion of the first bond shelf.

1 26. The method as recited in claim 25, wherein
2 the portion drilled in the first bond shelf is a notch.

1 27. The method as recited in claim 21, wherein
2 the portion of the first conductive strip is removed by
3 etching away a portion of the first conductive strip of the
4 first bond shelf.

1 28. The method as recited in claim 21, wherein

2 the package housing is provided by
3 forming a first conductive layer on a first dielectric
4 substrate,
5 placing a second dielectric substrate on the first conductive
6 layer of the first dielectric substrate, the second dielectric
7 substrate having a second conductive layer, and
8 etching the second conductive layer to form the first plurality
9 of bonding pads.

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1 29. The method as recited in claim 28, wherein
2 the first conductive layer forms the first conductor under the
3 first bond shelf.

1 30. The method as recited in claim 28, wherein
2 the etching of the second conductive layer to further form a
3 second conductor, and
4 the package housing has a second plurality of bonding pads
5 located on a second bond shelf, the second bond shelf having a
6 second edge, the package housing is further provided by
7 placing a third dielectric substrate on the second conductive
8 layer of the second dielectric substrate, the third dielectric
9 substrate having a third conductive layer, and
10 etching the third conductive layer to form a second plurality of
11 bonding pads, and

12 the method further includes
13 forming a second conductive strip along the second edge of the
14 second bond shelf, the second conductive strip wrapping around
15 the second edge of the second bond shelf from at least one of
16 the second plurality of bonding pads on the second bond shelf to
17 the second conductor under the second bond shelf.

1 31. The method as recited in claim 30, wherein
2 the second conductive layer forms the second conductor under the
3 second bond shelf.

1 32. The method as recited in claim 30, wherein
2 the second conductive strip is formed by plating a conductive
3 material onto the second edge.

1 33. The method as recited in claim 30, wherein
2 the second conductor under the second bond shelf is a power bus.

1 34. The method as recited in claim 30, wherein
2 the second conductor under the second bond shelf is a routing
3 trace.